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August 29, 1995

JAMES D. PLUMMER
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Reference:	AASERT Contract N00014-94-0748
Title:	"Sub Tenth Micron CMOS Devices - A Demonstration of the Virtual Factory Approach to New Structure Design"
P.I.:	James D. Plummer
Department:	Electrical Engineering
Period:	July 1, 1994 - June 30, 1997

Dear Ralph:

Enclosed are three (3) copies of our annual technical update on the above-named research grant, for the period July 1, 1994 - June 30, 1995. Also included is Exhibit C of the Reporting Form.

Sincerely,

James D. Plummer

Copy: Linden Clausen
Admin. Grants Officer
202 McCullough Building
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IN REPLY REFER TO:

4330
ONR 247
11 Jul 97

From: Director, Office of Naval Research, Seattle Regional Office, 1107 NE 45th St., Suite 350, Seattle, WA 98105
To: Defense Technical Center, Attn: P. Mawby, 8725 John J. Kingman Rd., Suite 0944, Ft. Belvoir, VA 22060-6218

Subj: RETURNED GRANTEE/CONTRACTOR TECHNICAL REPORTS

1. This confirms our conversations of 27 Feb 97 and 11 Jul 97. Enclosed are a number of technical reports which were returned to our agency for lack of clear distribution availability statement. This confirms that all reports are unclassified and are "APPROVED FOR PUBLIC RELEASE" with no restrictions.

2. Please contact me if you require additional information. My e-mail is *silverr@onr.navy.mil* and my phone is (206) 625-3196.

ROBERT J. SILVERMAN

AASERT Project N00014-94-1-0748

"Sub Tenth Micron CMOS Devices - A Demonstration of the Virtual Factory Approach to New Structure Design"

Principal Investigator: Prof. J. D. Plummer
Graduate Student: Chris Auth

Annual Technical Report
July 1, 1994 - June 30, 1995

The parent program "Semiconductor Manufacturing For the 21st Century" has focused on showing the power of a "Virtual Factory" operating in parallel with a computer controlled "Programmable Factory". This project is exploring the use of advanced TCAD simulation tools to design a candidate 21st century MOS device - a fully-depleted surrounding gate vertical MOSFET with self-aligned drain contact. The structure is a vertical MOSFET built in an etched silicon pillar. It has been built at much larger dimensions (1 micron) and shows significant promise of being scalable to very small dimensions. The project uses the "Virtual Factory" to design the device and before actual fabrication in the lab at Stanford to test the correspondence between the simulation results and the actual experimental results.

In the past year the fabrication of the vertical MOSFETs was started and completed. The process began with the anticipation of only fabricating optically defined pillars. Fortunately the direct write e-beam system became operable for a short time and approximately half of the wafers were exposed utilizing the e-beam. This produced very good results with pillar widths less than 0.1 micron observed. The actual etch profile of these pillars was also better than expected.

With the actual etch profiles the remaining process was re-simulated and refined because the actual etch profile has an impact on the gate and source/drain implant steps. Before the e-beam system came on-line the possibility of oxidizing optically defined pillars was investigated. Simulations were compared with actual oxidations carried out in the lab. The effects of stress in the oxidation process were shown by SUPREM-4 as the reason that the resulting profiles were unsatisfactory.

The etching of the gate was completed with satisfactory results. The selectivity of the polysilicon to the oxide etch was approximately 15. Some short loop processing was undertaken to look for ways to improve this figure. The culprit was shown to be carbon from the photoresist. An attempt to use an oxide mask failed suggesting that the oxide (LTO) also had carbon contamination.

The next step was the implantation of the source and drain regions. SUPREM-4 simulations were carried out using the actual gate etch profiles to refine the implant angle and the subsequent anneal step.

The final critical step was the planarization of the wafer in order to make the overlapping drain contact without shorting it to the gate. The base process was a resist-etch-back scheme with a non-selective etch. This gave satisfactory results but the possibility of using SOG planarization is being looked into. Pillar widths of down to 0.1um were built. Working transistors illustrated the feasibility of the process and measurements of subthreshold slope showed values down to the ideal value of 60mV/dec. There are still a few ebeam defined wafers remaining and these will be processed this fall to obtain more data with different pillar heights.

Finally, device simulations showing the transconductance and short channel behavior of these devices have also been made. These simulations look at the effect of the various parameters on the devices, including gate oxide thickness, doping and pillar width. The simulations shown a surprisingly sharp decrease of the slope as the pillar width decreased. These simulations are to be compared to traditional planar MOSFETs and SOI devices.

This next year will hopefully see the conclusion of the e-beam defined device run. From these results the full CMOS process will be refined and a second run using this full CMOS process will be started.

FORM A2-2

AUGMENTATION AWARDS FOR SCIENCE & ENGINEERING RESEARCH TRAINING (AASERT) REPORTING FORM

The Department of Defense (DOD) requires certain information to evaluate the effectiveness of the AASERT program. By accepting this Grant Modification, which bestows the AASERT funds, the Grantee agrees to provide the information requested below to the Government's technical point of contact by each annual anniversary of the AASERT award date.

1. Grantee identification data: (R & T and Grant numbers found on Page 1 of Grant)

a. Stanford
University Name

b. N00014-94-0748
Grant Number

c. 3333002aas01
R & T Number

d. J.D. Plummer
P.I. Name

e. From: 7/1/94 - To: 6/30/95
AASERT Reporting Period

NOTE: Grant to which AASERT award is attached is referred to hereafter as "Parent Agreement."

2. Total funding of the Parent Agreement and the number of full-time equivalent graduate students (FTEGS) supported by the Parent Agreement during the 12-month period **prior to** the AASERT award date.

a. Funding: $ 2,900,000

b. Number FTEGS: 25

3. Total funding of the Parent Agreement and the number of FTEGS supported by the Parent Agreement during the current 12-month reporting period.

a. Funding: $ 950,000 (Parent contract ended 1/31/95)

b. Number FTEGS: 25

4. Total AASERT funding and the number of FTEGS and undergraduate students (UGS) supported by AASERT funds during the current 12-month reporting period.

a. Funding: $ 82,080

b. Number FTEGS: 1

c. Number UGS: 0

VERIFICATION STATEMENT: I hereby verify that all students supported by the AASERT award are U.S. citizens.

James D. Plummer
Principal Investigator

8/29/95
Date